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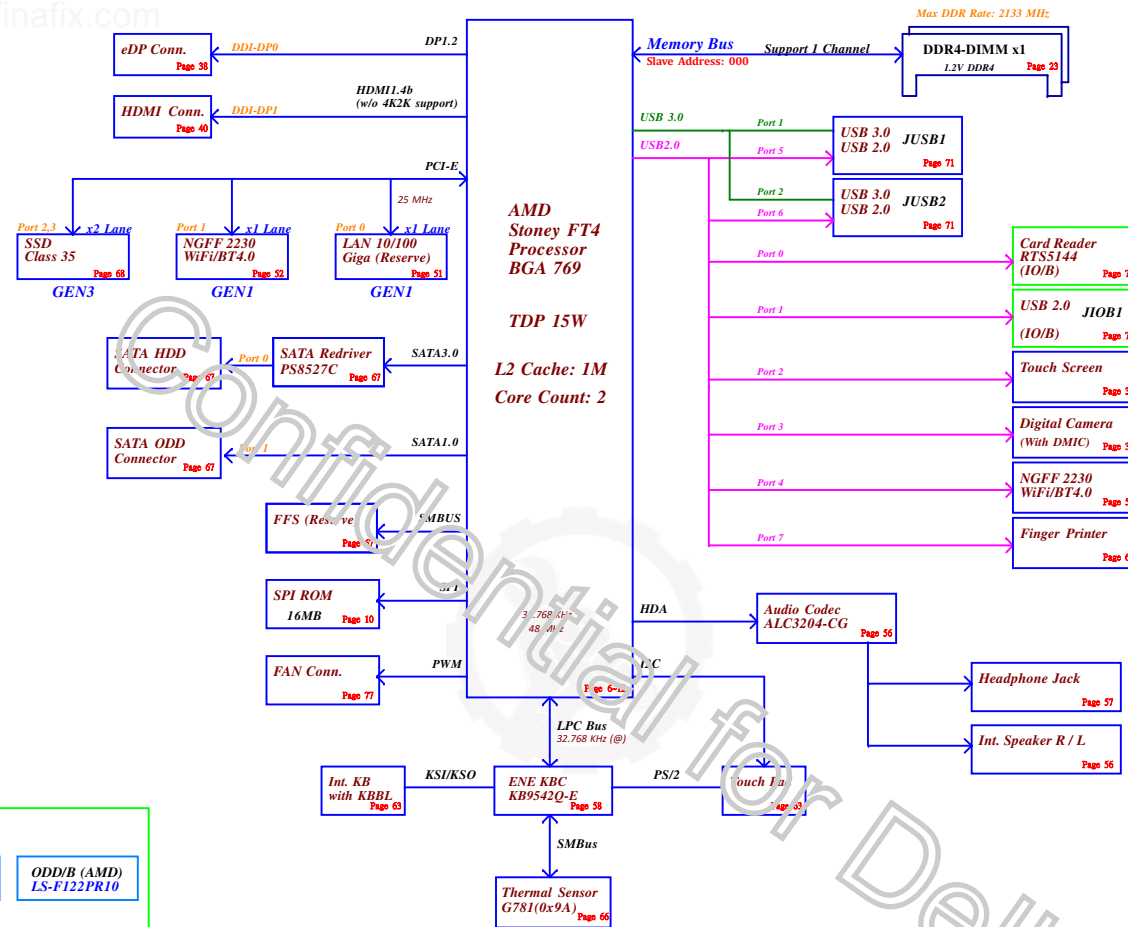
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Schematic Document

AMD Stoney Ridge

2018-05-21 Rev: 1.0 (A00)

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SUB-BOARDS



Board ID Table for AD Channel:

Vcc	3.3V +/- 1%
Ra[RE5]	100K +/- 1%

Board ID	Rb[RE9]	VAD_min	VAD_typ	VAD_max	EC AD3
0	0 ohm	0.000V	0.000V	0.300V	0x00 - 0x13
1	12K +/- 1%	0.347V	0.354V	0.360V	0x14 - 0x1E
2	15K +/- 1%	0.423V	0.430V	0.436V	0x1F - 0x25
3	20K +/- 1%	0.541V	0.550V	0.559V	0x26 - 0x30
4	27K +/- 1%	0.691V	0.702V	0.713V	0x31 - 0x3A
5	33K +/- 1%	0.807V	0.819V	0.831V	0x3B - 0x45
6	43K +/- 1%	0.978V	0.992V	1.006V	0x46 - 0x54
7	56K +/- 1%	1.169V	1.185V	1.200V	0x55 - 0x64
8	75K +/- 1%	1.398V	1.414V	1.430V	0x65 - 0x76
9	100K +/- 1%	1.634V	1.650V	1.667V	0x77 - 0x87
10	130K +/- 1%	1.849V	1.865V	1.881V	0x88 - 0x96
11	160K +/- 1%	2.015V	2.031V	2.046V	0x97 - 0xA4
12	200K +/- 1%	2.185V	2.200V	2.215V	0xA5 - 0xAF
13	240K +/- 1%	2.316V	2.329V	2.343V	0xB0 - 0xB7
14	270K +/- 1%	2.395V	2.408V	2.421V	0xB8 - 0xBF
15	330K +/- 1%	2.521V	2.533V	2.544V	0xC0 - 0xC9
16	430K +/- 1%	2.667V	2.677V	2.687V	0xCA - 0xD4
17	560K +/- 1%	2.791V	2.800V	2.808V	0xD5 - 0xDD
18	750K +/- 1%	2.905V	2.912V	2.919V	0xDE - 0xF0
19	NC	3.000V	3.300V	3.300V	0xF1 - 0xFF

BOARD ID Table:

Board ID	Definition
0	N3V3 MLK STR UMA <EVT>
1	N3V3 MLK STR UMA <DVT1>
2	N3V3 MLK STR UMA <DVT2>
3	N3V3 MLK STR UMA <PVT>
4	N/A
5	N/A
6	N/A
7	N/A
8	N/A
9	N/A
10	N/A
11	N/A
12	N/A
13	N/A
14	N/A
15	N/A
16	N/A
17	N/A
18	N/A
19	N/A

Symbol Note:

 : Means Digital Ground

 : Means Analog Ground

SMBUS Control Table:

	SOURCE	BATT	Charger	Thermal Sensor	Touch Pad	DIMM	FFS
EC_SMB_CR1 EC_SMB_DA1	KB9542	V	V				
EC_SMB_CR2 EC_SMB_DA2	KB940			V			
TP_CLK TP_DATA	KB9542				V		
APU_SCLK0 APU_SDATA0	APU					V	V
APU_SIC APU_SID	APU			V			

Voltage Rails

Power Plane	Description	S1	S2	S2/S3
+19V_VIN	Adapter power supply	N/A	N/A	N/A
+17.4V_BATT++	Battery power supply	N/A	N/A	N/A
+19VB	AC or DC for power circuit	N/A	N/A	N/A
+5VALW	System +5VALW power rail	ON	ON	ON
+3VALW	System +3VALW power rail	ON	ON	ON*
+1.8V_ALW	System +1.8VALW power rail	ON	ON	ON*
+0.95VALW	System +0.95VALW power rail	ON	ON	ON*
+0.775VALW	System +0.775VALW power rail	ON	ON	ON*
+1.2V_DDR	DDR4 +1.2V power rail	ON	ON	OFF
+0.6V_DDR_VTT	DDR4 +0.6V power rail	ON	OFF	OFF
+2.5V_MEM	DDR4 +2.5V power rail	ON	ON	OFF
+5VS	System +5VS power rail	ON	OFF	OFF
+3VS	System +3VS power rail	ON	OFF	OFF
+1.8VS	System +1.8VS power rail	ON	OFF	OFF
+0.95VS	System +0.95VS power rail	ON	OFF	OFF
+APU_CORE	Core voltage for APU	ON	OFF	OFF
+APU_CORE_NB	Core NB voltage for APU	ON	OFF	OFF
+VDDCR_FCH_ALW	S5 supply voltage for the FCH core logic	ON	OFF	OFF
+3VLP	+19VB to +3VLP power rail for suspend power	ON	ON	ON
+RTCVCC	RTC power	ON	ON	ON
+0.95VS_APU_GFX	PCIe GPP, PCIe GFX, DP and SATA PHY logic power rail for APU	ON	OFF	OFF
+3VS_APU	+3VS power rail for APU	ON	OFF	OFF

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF

HS I/O

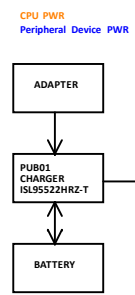
USB3.0

Port 0	---
Port 1	USB3 Connector Port 1
Port 2	USB3 Connector Port 2
USB2.0	
Port 0	Card Reader (IO/B)
Port 1	USB2 Connector Port (IO/B)
Port 2	Touch Screen
Port 3	Camera
Port 4	WLAN
Port 5	USB2 Connector Port 1
Port 6	USB2 Connector Port 2
Port 7	Finger Printer
SATA	
Port 0	HDD
Port 1	ODD
Display(DP)	
Port 0	eDP (Lan0/Lan1)
Port 1	HDMI (Lan0/Lan1/Lan2/Lan3)
Port 2	---

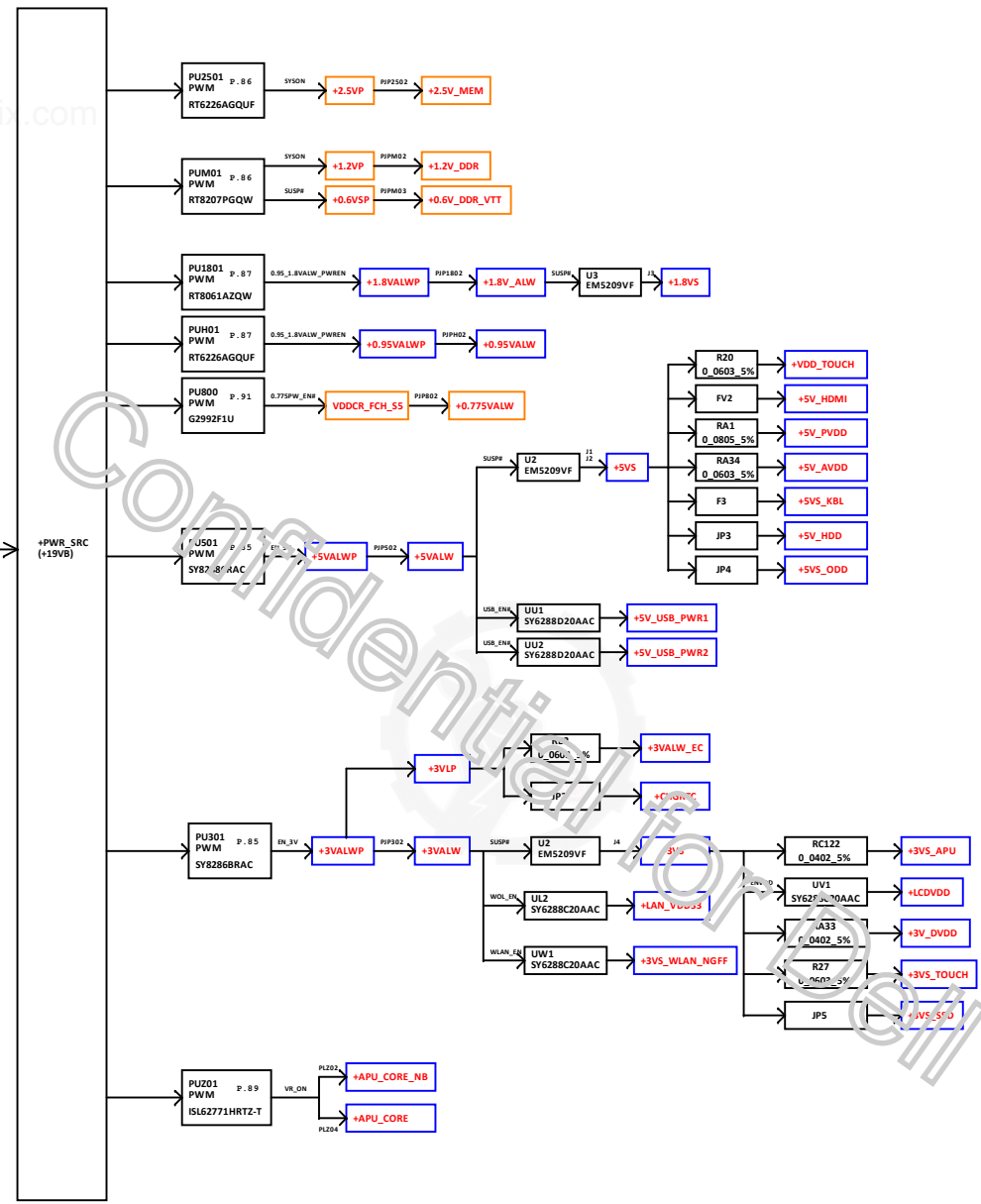
Clock Signal

GFX_CLK	---
GPP_CLK0	LAN
GPP_CLK1	WLAN
GPP_CLK2	NVMe SSD
GPP_CLK3	---
PCI Express(GFX)	
Lane 0	---
Lane 1	---
Lane 2	---
Lane 3	---
PCI Express(GPP)	
Lane 0	LAN
Lane 1	WLAN
Lane 2	NVMe SSD
Lane 3	NVMe SSD

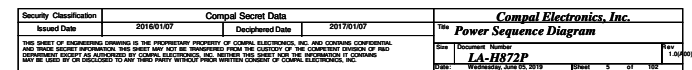
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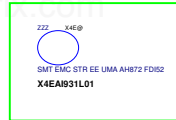
CPU PWR
Peripheral Device PWR



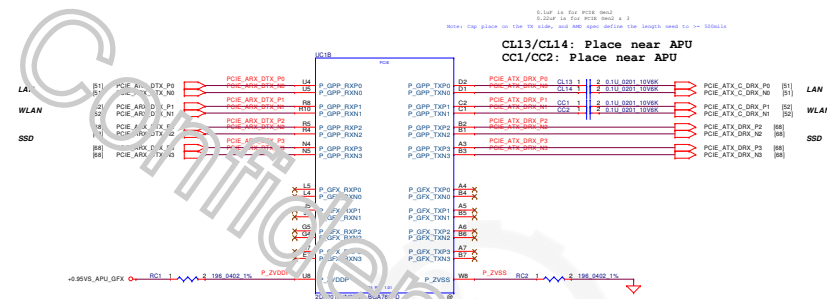
2019/4/26



EMC X4E for BOM control:

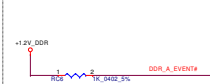


15W APU R1 P/N		15W APU R3 P/N	
UC1	<p>(NPI used D Mark P/N)</p> <p>SA00080GTL</p> <p>As, R1p</p> <p>S IC A6-9225 AMR025AYN23AC 2.6G APU A311</p>	UC1	<p>SA00080GTL</p> <p>As, R3p</p> <p>S IC A6-9225 AMR025AYN23AC 2.6G APU A311</p>
UC1	<p>(NPI used D Mark P/N)</p> <p>SA00080GL</p> <p>As, R1p</p> <p>S IC A6-9425 AMR042AYN23AC 3.1G APU A311</p>	UC1	<p>SA00080GL</p> <p>As, R3p</p> <p>S IC A6-9425 AMR042AYN23AC 3.1G APU A311</p>



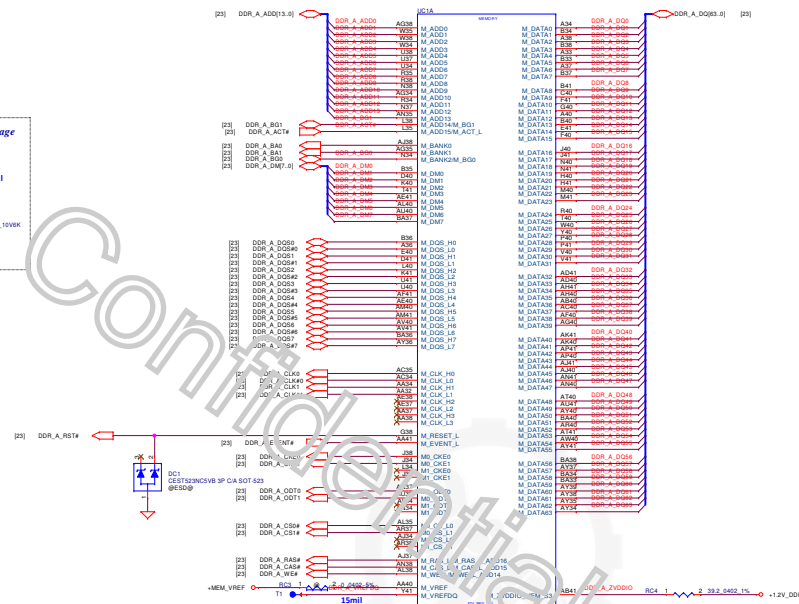
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EVENT# pull high

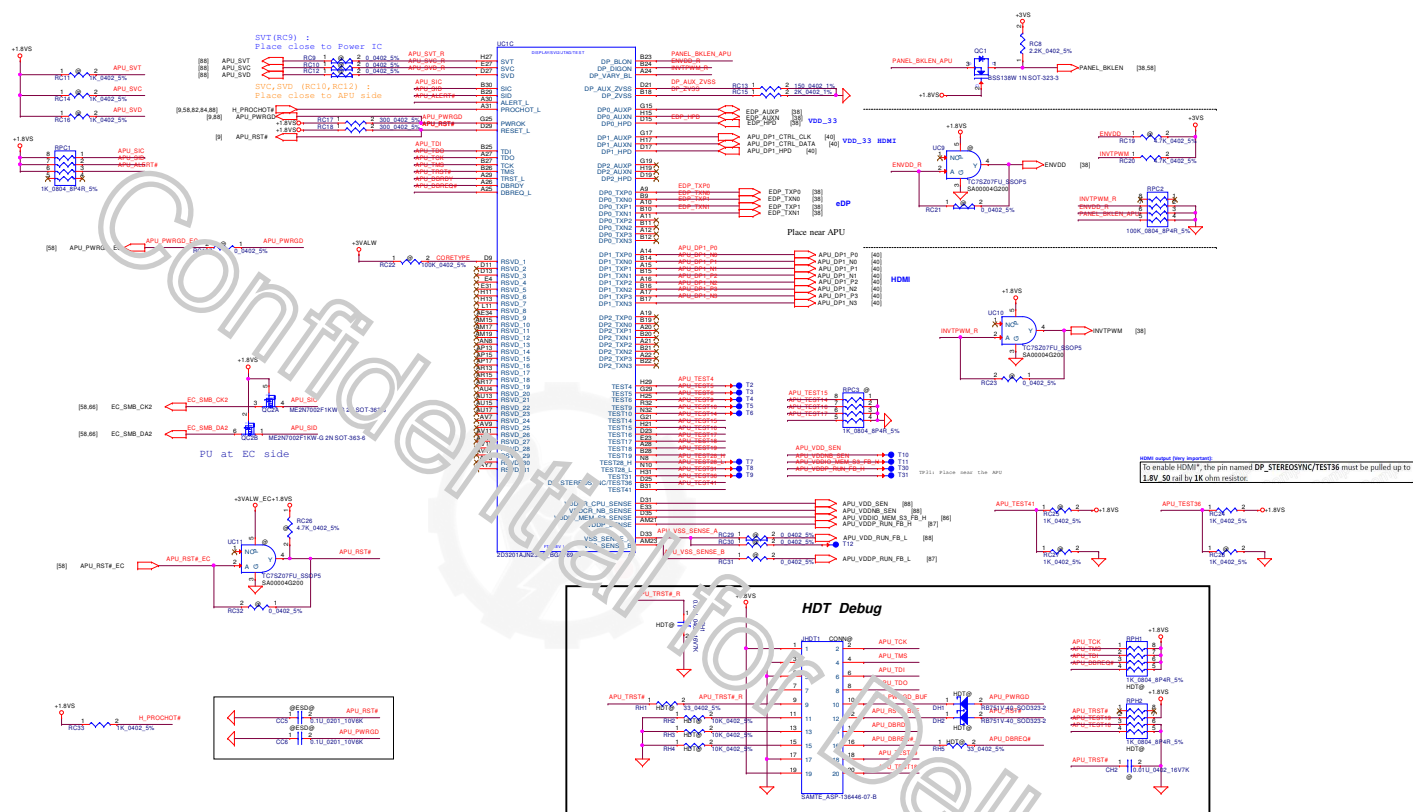


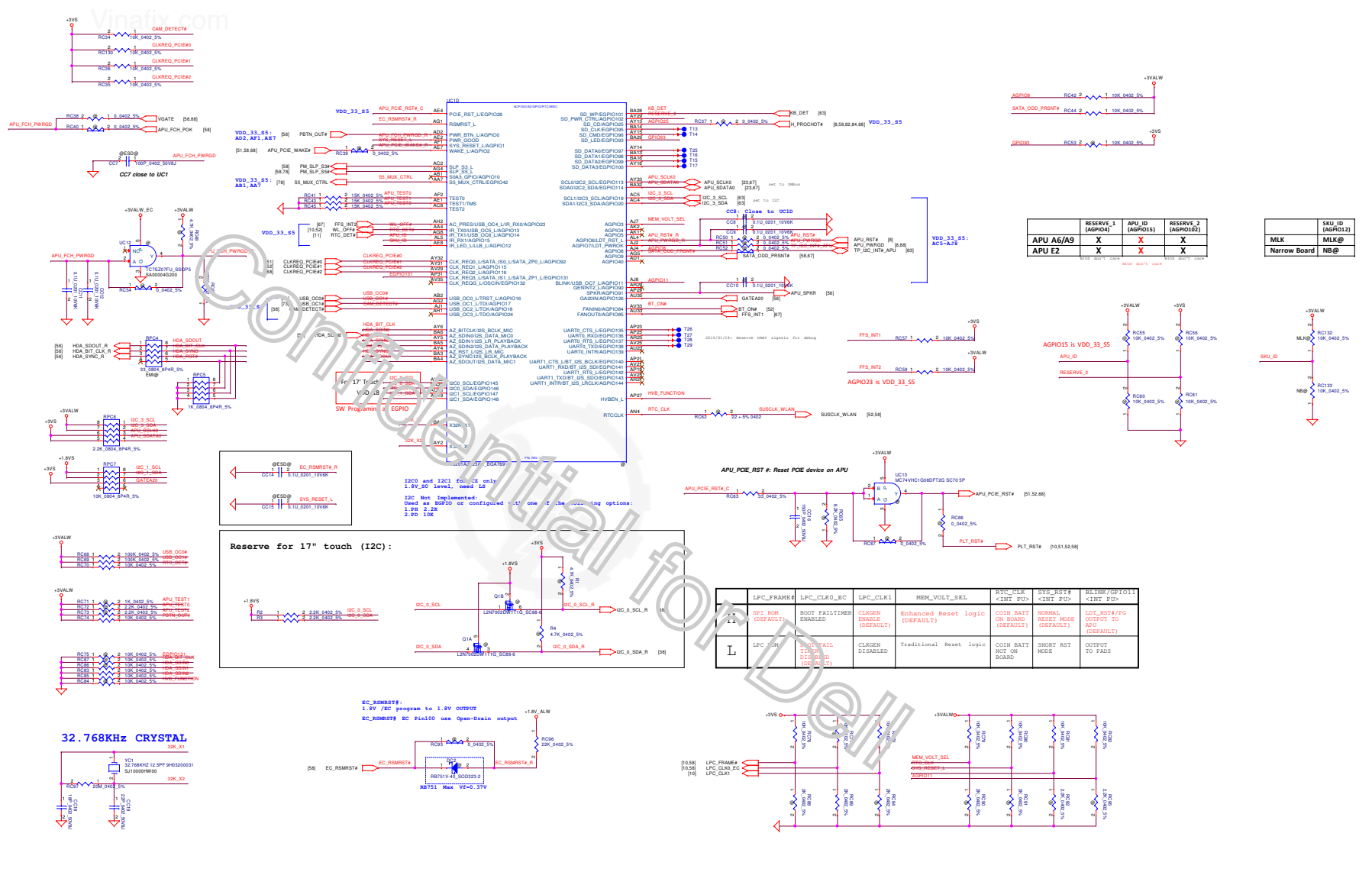
+1.2V_DDR

0.6V reference voltage



Place them close to A#1 within 1"

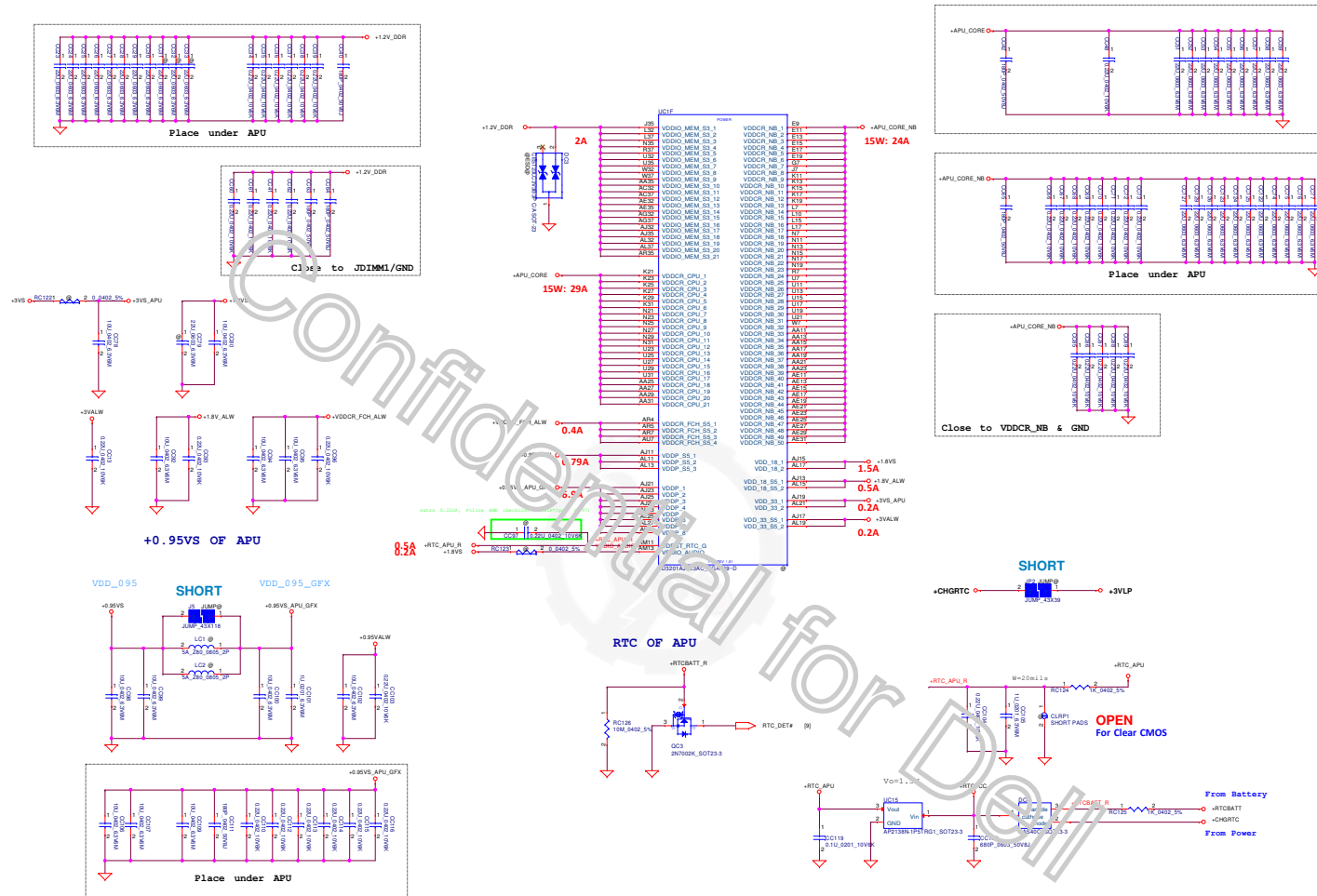


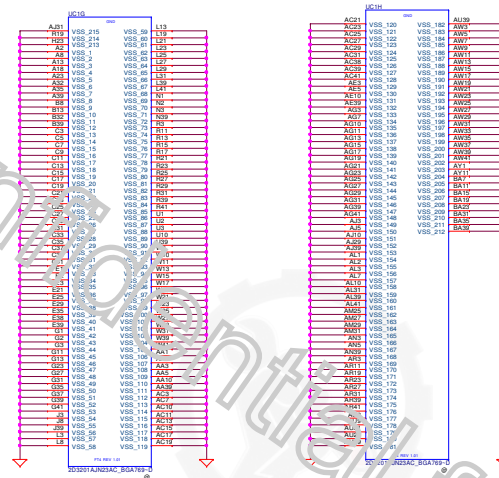


	RESERVE 1 (AP004)	APU_ID (AP001)	RESERVE 2 (AP002)
APU A6/A9	X	X	X
APU E2	X	X	X

	SKU_ID (AP002)
MLK	MLK@
Narrow Board	NB@

	LPC_FRAME#	LPC_CLK0_EC	LPC_CLK1	MEM_VOLT_SEL	RTC_CLK <INT PU>	SYS_RST# <INT PU>	BLINK/OP011 <INT PU>
1	SP1 ROM (DEFAULT)	BOOT FAILTIMER	CLKEN (DEFAULT)	Enhanced Reset logic (DEFAULT)	COIN BATT ON BOARD (DEFAULT)	NORMAL RESET MODE (DEFAULT)	LD1_RST#/PG OUTPUT TO APU (DEFAULT)
L	LPC (CH)	BOOT FAIL (DEFAULT)	CLKEN (DEFAULT)	Traditional Reset logic	COIN BATT NOT ON BOARD	SHORT RST MODE	OUTPUT TO PAUD





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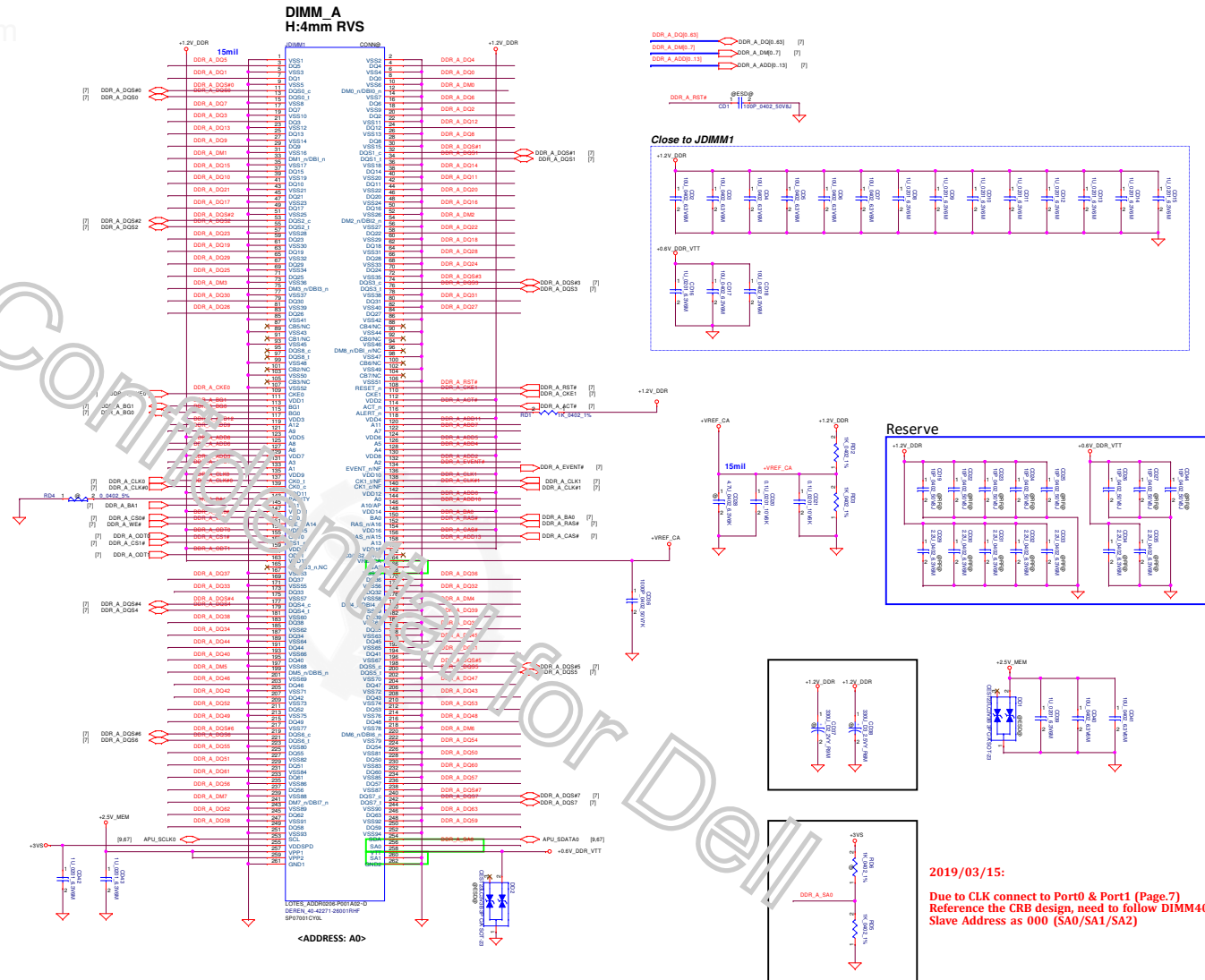
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2019/03/15:
Due to CLK connect to Port0 & Port1 (Page.7)
Reference the CRB design, need to follow DIMM400 setting :
Slave Address as 000 (SA0/SA1/SA2)

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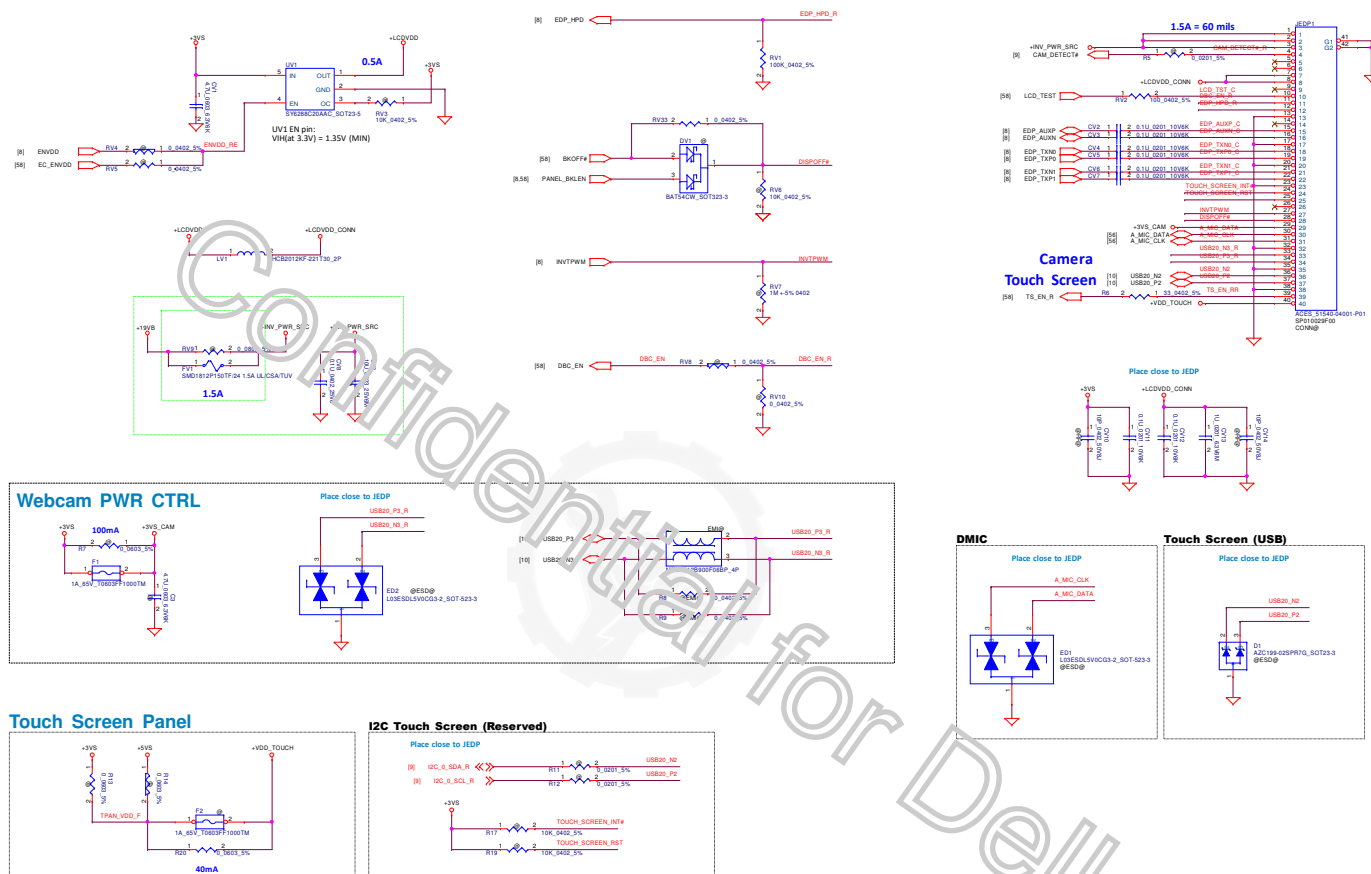
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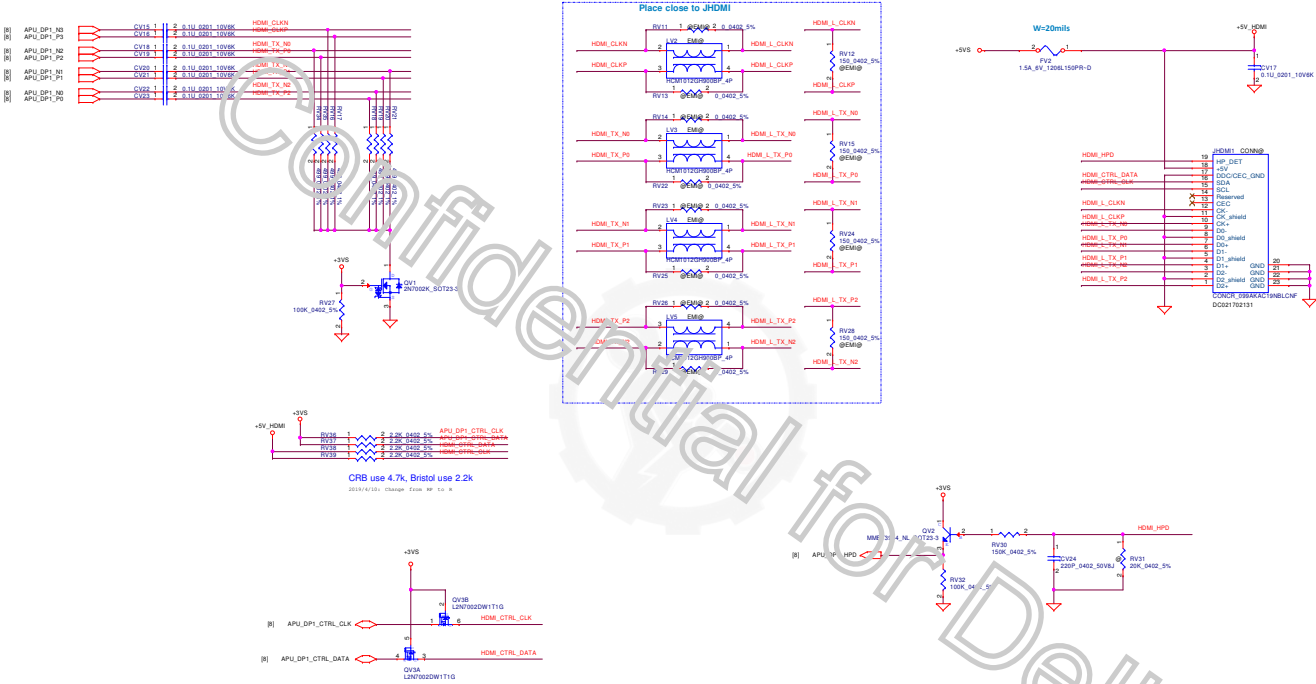
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#58	ROYALTY HDMI LOGO
Unit: Millimeter	Scale: 1:1
Model: 00000000000000000000	Rev: 0



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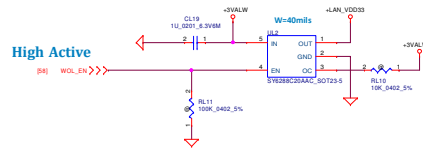
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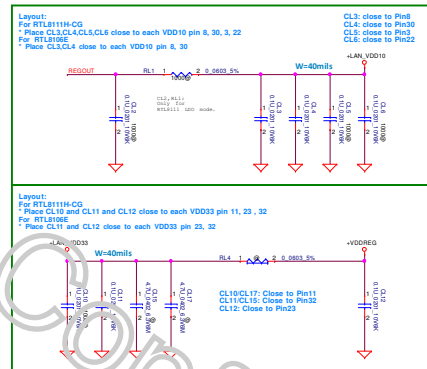
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+LAN_VDD33 Rising time (10%-90%)
Need to: >0.5mS & <100mS.



	1.0V Source	RL1	CL2	CL5	CL6	CL10	CL12
RTL8111H-CG RTL8111G-CG2 (71.08111 U03)	LDO	O	O	O	O	O	X
RTL8106E-CG (071.08106.0003)	LDO	X	X	X	X	X	O

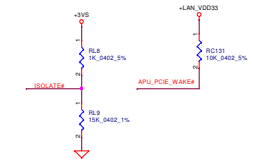
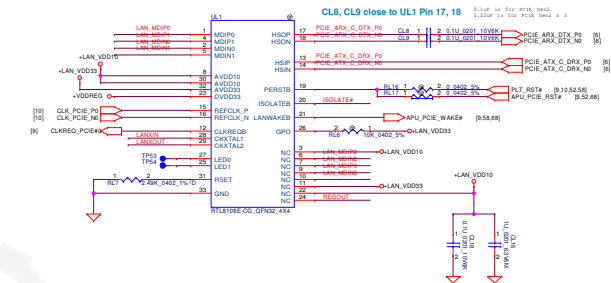
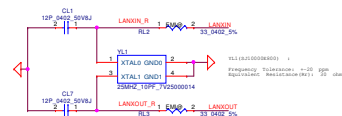


LAN CHIP 10/100/1000

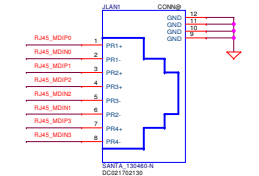
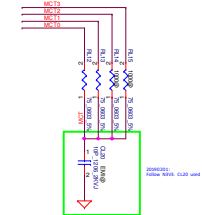
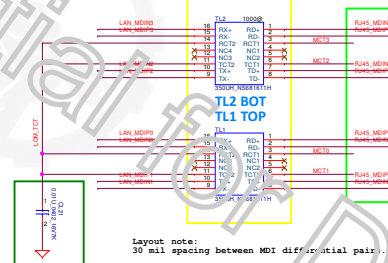
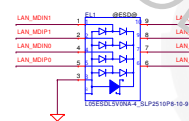
VOL1000-10	RTL8111H-CG
0000000000	0000000000
LDO: 1000	LDO: 1000
10/1000	10/1000/10000



Note: Giga LAN (Reserve)



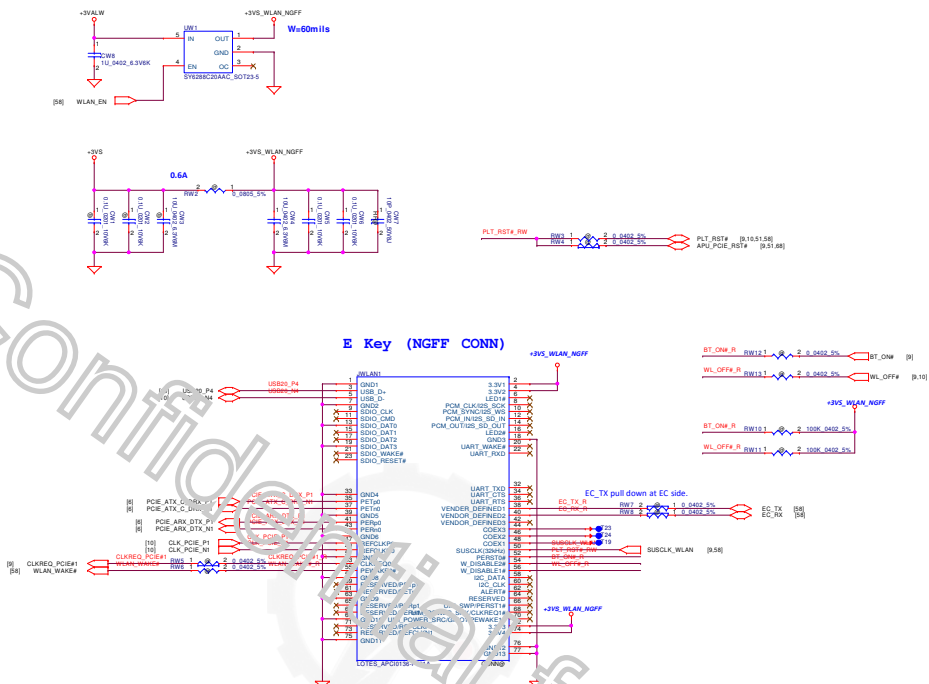
LAN Transformer 10/100M x2

Layout note:
30 mil spacing between MDI differential pair.Main:
SP050009800, 5 XFORM, NS681611H LDO
2nd:
SP050006W00, 5 XFORM, HD-245 10/100 PC CANAL

Follow Reference Schematic 0.01uF-0.4uF

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Title LAN RTL8111/RTL8106		Rev LA-H872P
Date Wednesday, June 20, 2018		Sheet 51 of 100

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DATE: Wednesday, June 01, 2017					Page 1 of 1

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				LA-H872P
				Page 10 of 102

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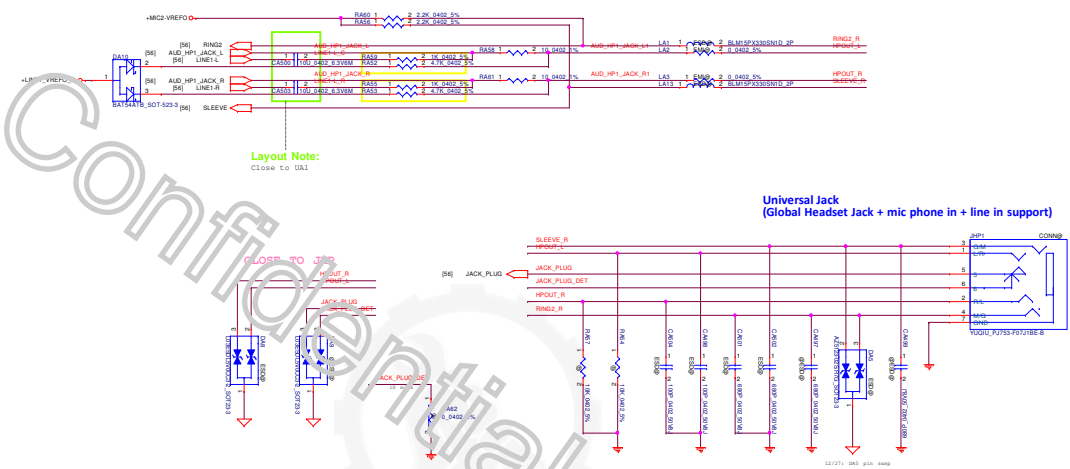
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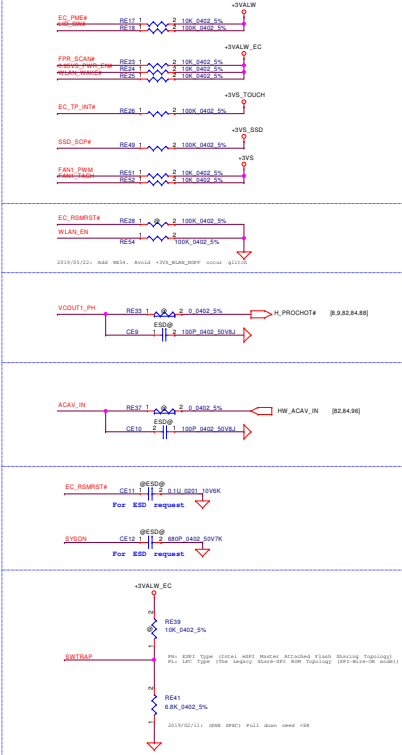
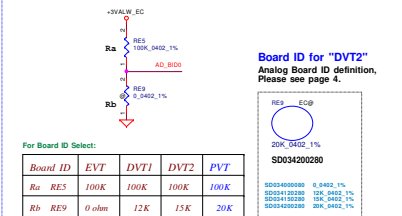
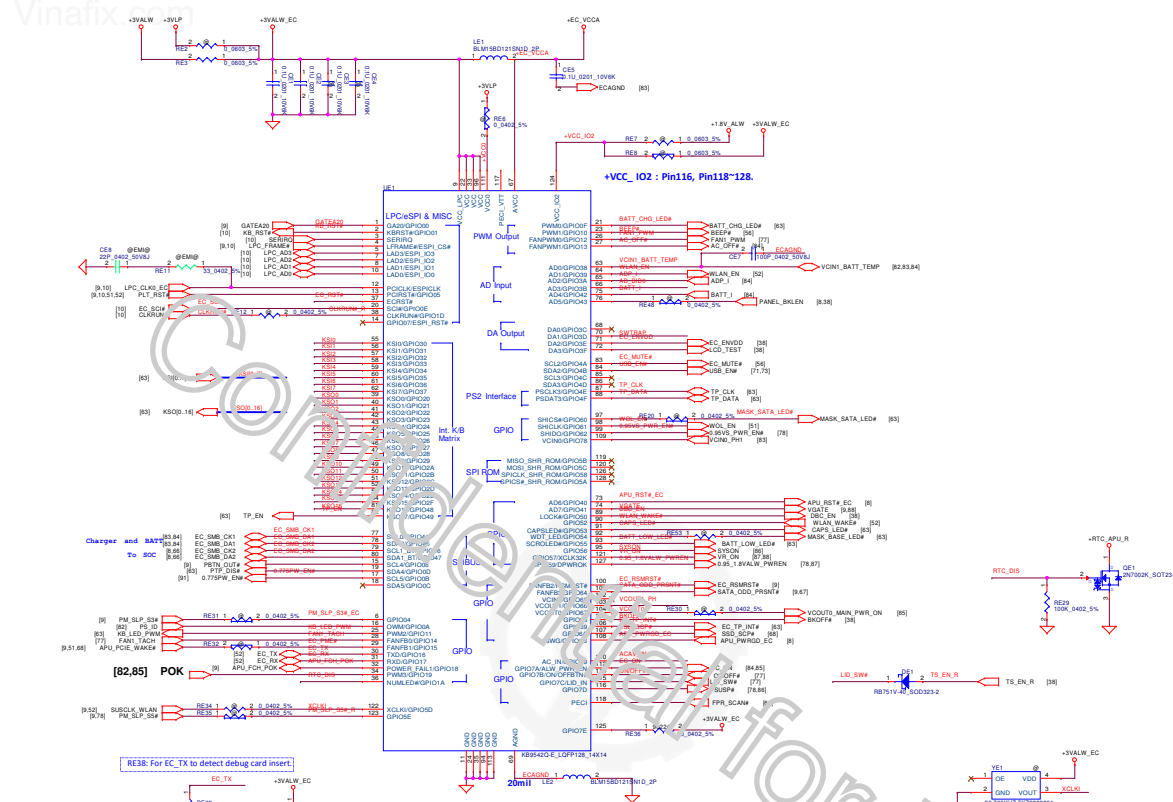
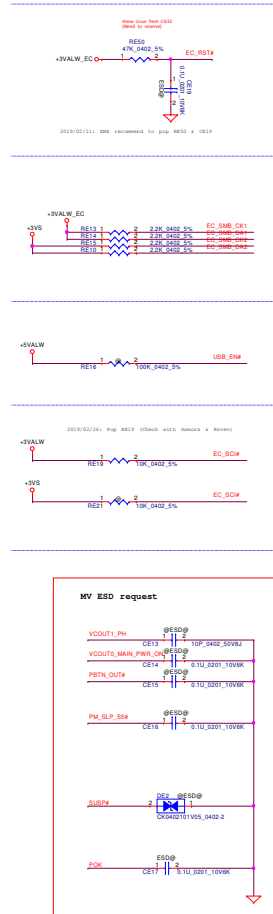
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2019/03/21:
Change UE1 from B to E version.



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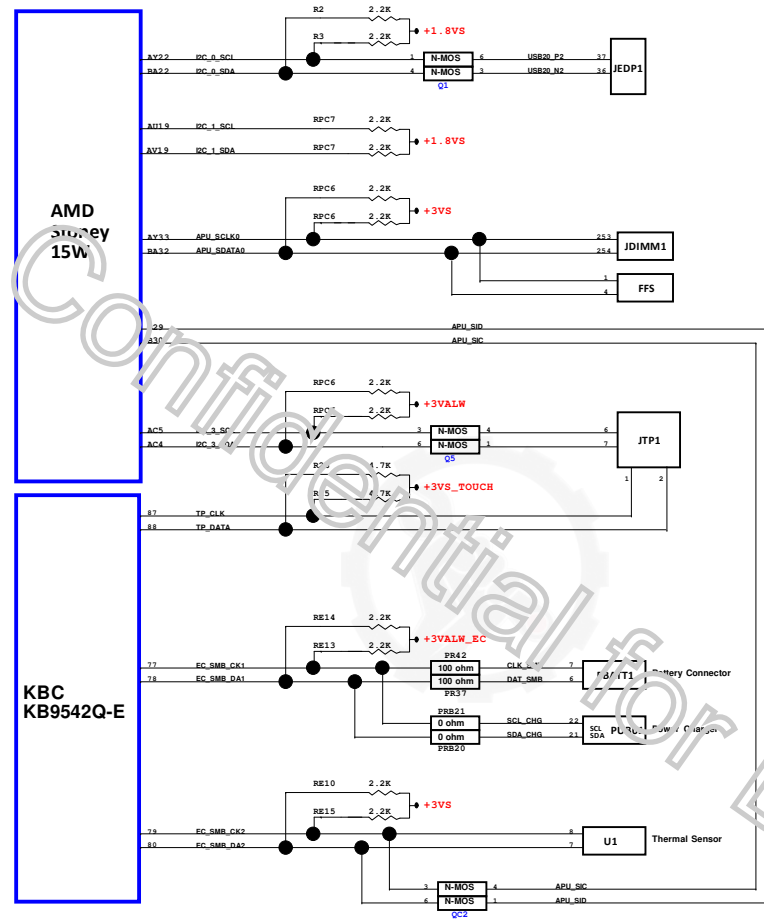
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SMBus Block Diagram 2019/01/21: Finished.

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				LA-H872P		
				Date	Issued	
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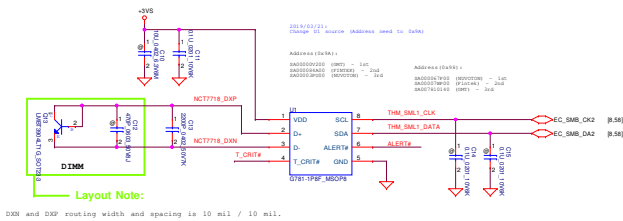
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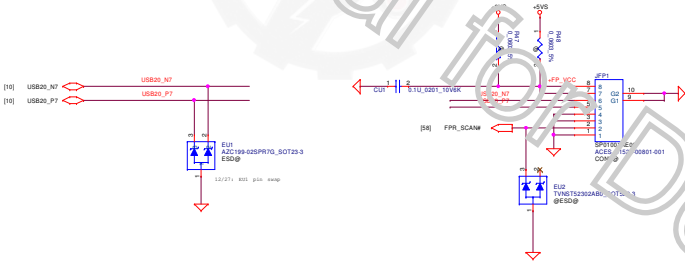
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Wednesday, June 01, 2016		001		01 of 102	

Main Func = Thermal Sensor

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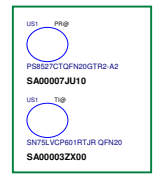
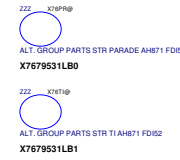


Main Func = Finger Printer

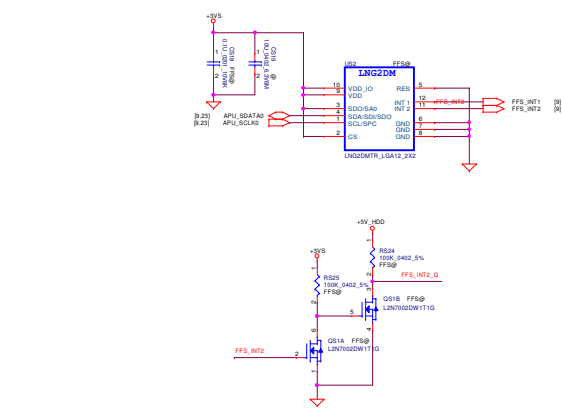


Main Func = HDD

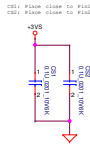
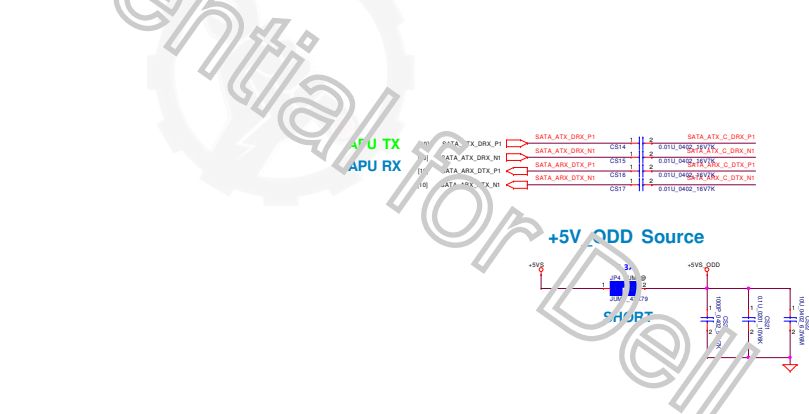
SATA X76 for BOM control:



Main Func = FFS

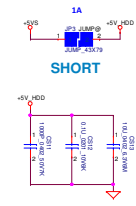


Main Func = ODD

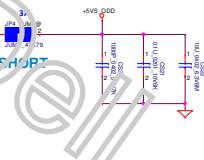


2019/02/25: Change R519,R521 BOM structure to TI@

+5V_HDD Source



+5V_ODD Source



8.3.2 Output De-Emphasis

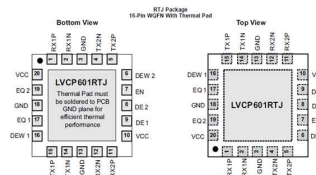
The SN75LVCP601 device provides the de-emphasis settings shown in Table 1. De-emphasis control is independent for each channel, controlled by the DE1 and DE2 pin settings as shown in Table 1. The reference for the de-emphasis settings available in the device is the transition bit amplitude for each given configuration; this transition bit amplitude is different at 0 dB than the -2dB and -4dB settings by design. DEW1 and DEW2 control the DE durations for channels one and two, respectively. Table 1 lists the recommended settings for these control pins. Output de-emphasis is capable of supporting FRM trace at the output anywhere from 2 in. (5.1 cm) to 12 in. (30.5 cm) at SATA 3G/6G speed.

Table 1. TX and RX EQ and DE Pulse-Duration Settings

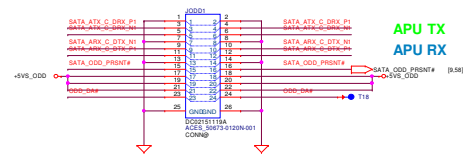
DE1 OR DE2	CH1 OR CH2 DE EMPHASIS (dB at 6 Gbps)	EQ1 OR EQ2	CH1 OR CH2 Equalization (dB at 6 Gbps)	PL RS19 / RS21
NC (default)	-4	NC (default)	0	PH RS10 / RS11
0	0	0	7	
1	-2	1	14	
DEW1 OR DEW2	DE WIDTH FOR CH1/CH2			
0	De-emphasis pulse duration, short			
1 (default)	De-emphasis pulse duration, long			

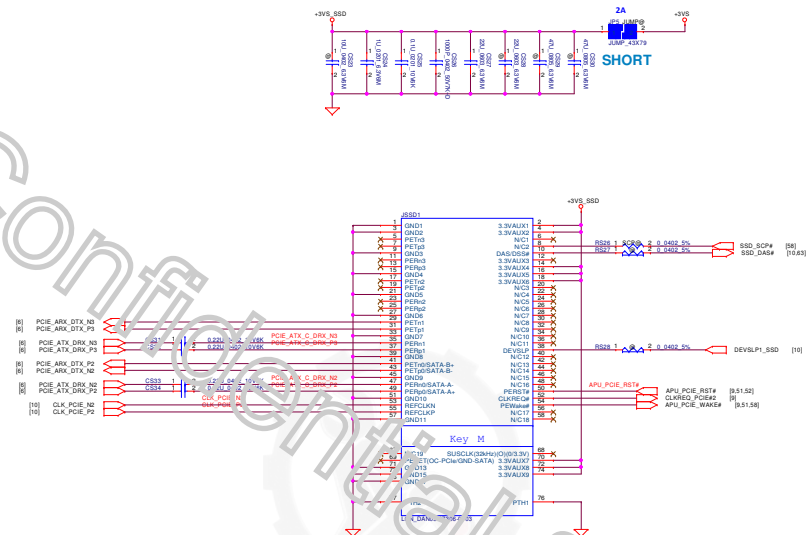
SN75LVCP601

5 Pin Configuration and Functions



SATA ODD Connector (FFC Type)





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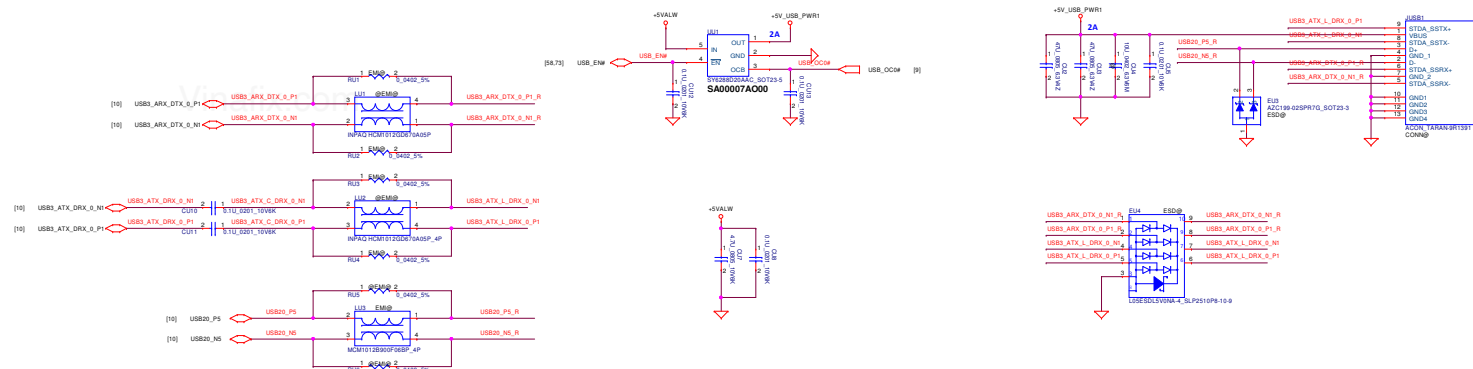
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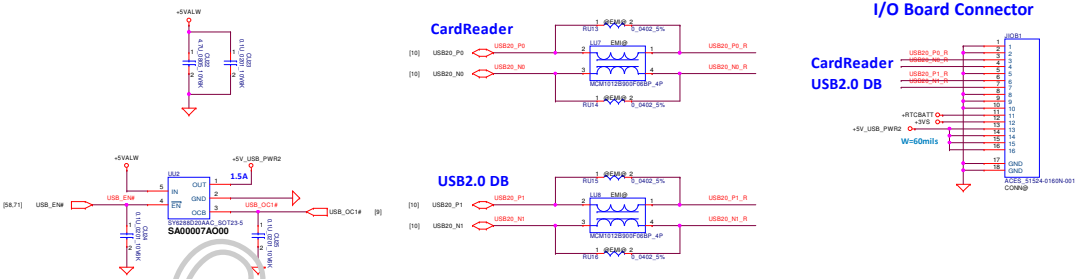
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LA-H872P		Rev. 1.0/001	Page 70	of 102

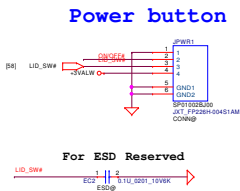
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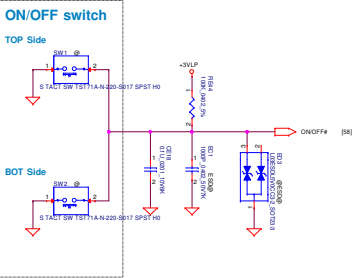
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Main Func = POWER BTN

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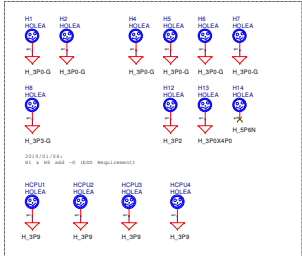


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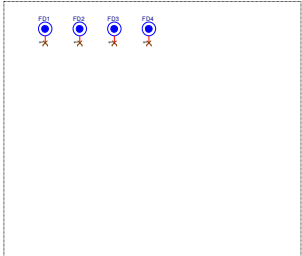


Main Func = Screw Hole

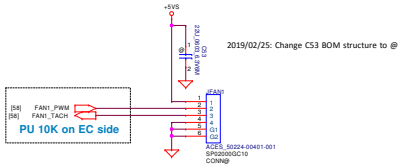
Screw Hole



FD



Main Func = FAN Control

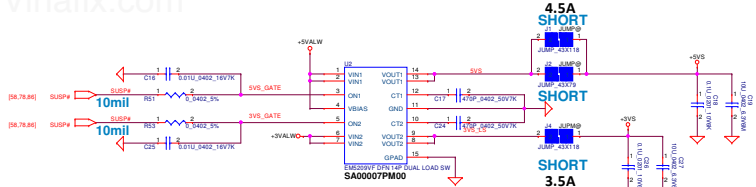


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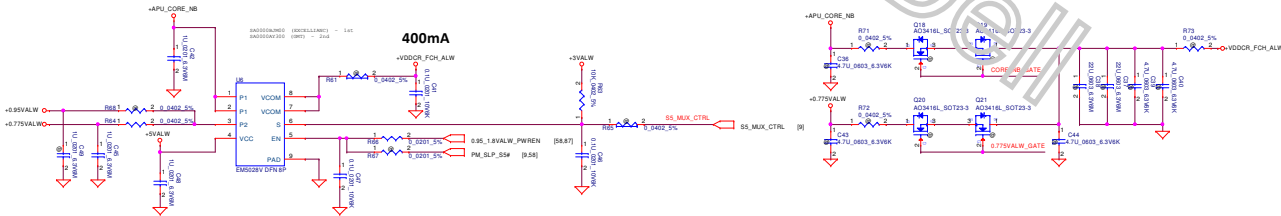
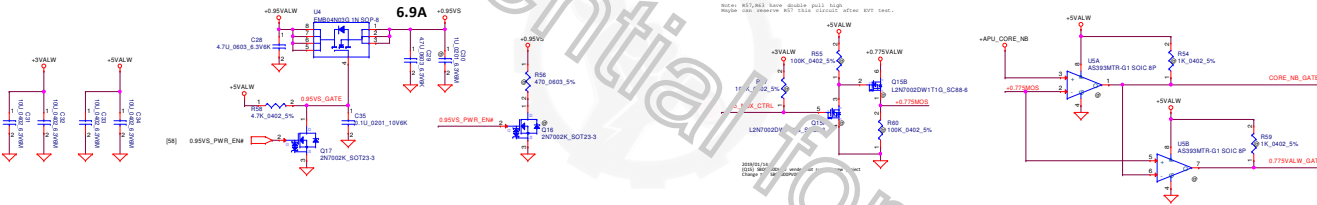
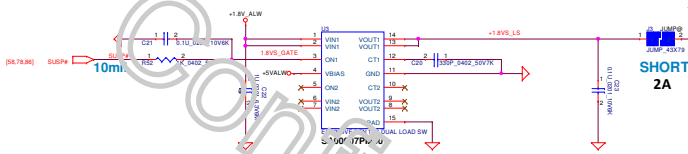
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LA-H872P	PCB 20F LA-H872P REV0 M/B 3
Part Number	Description
LA-H872P	PCB 20F LA-H872P REV0 M/B 3
Part Number	Description
LA-H872P	PCB 20F LA-H872P REV0 M/B 3
Part Number	Description
LA-H872P	PCB 20F LA-H872P REV0 M/B 3

+5VS and +3VS Switch

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+1.8VS Switch



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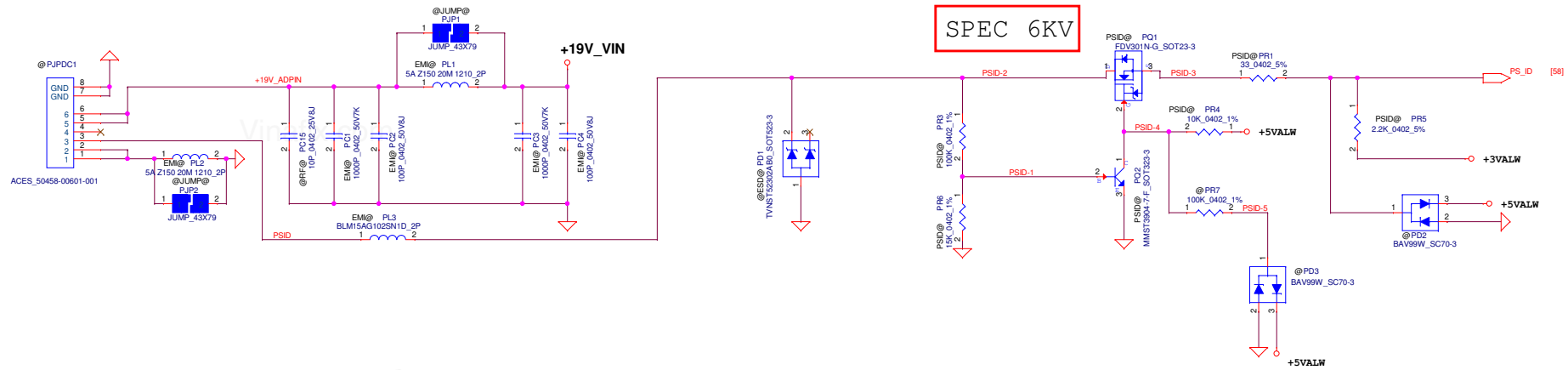
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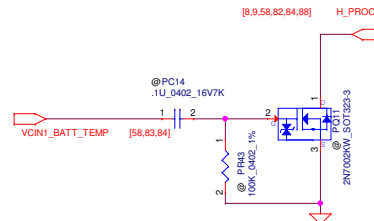
		
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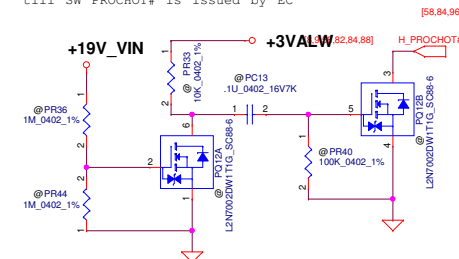
Adapter protection

if battery removed, adaptor only,
then trigger the H_PROCHOT#,
keep it in BOM since battery can not
be removed by end user

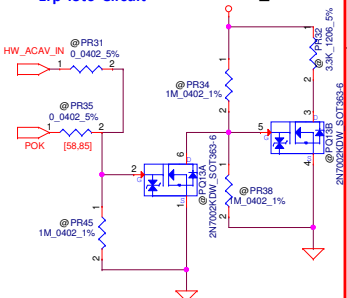


Battery protection

asserts H_PROCHOT# when adaptor is
unplugged, keep low for 10ms
till SW_PROCHOT# is issued by EC



Erp lot6 Circuit



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Compal Electronics, Inc.

PWR_DCIN/BATT_CONN/OTP

LA-H872P

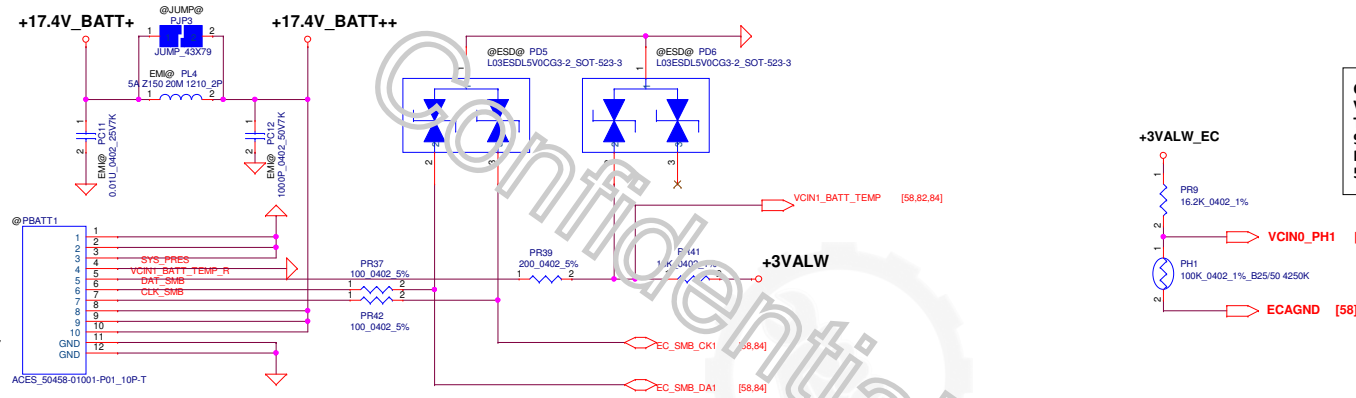
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Battery Bot Side

PIN1 GND
PIN2 GND
PIN3 GND
PIN4 SYS_PRES
PIN5 BATT_PRS
PIN6 DAT_SMB
PIN7 CLK_SMB
PIN8 Batt+
PIN9 Batt+
PIN10 Batt+
SP021412220

ACES_50458-01001-P01_10P-T



CPU thermal protection
VCIN0_PH
Trig = 1V
92 +/- 3 degree C
Recover = 2.016V
50 +/- 3 degree C

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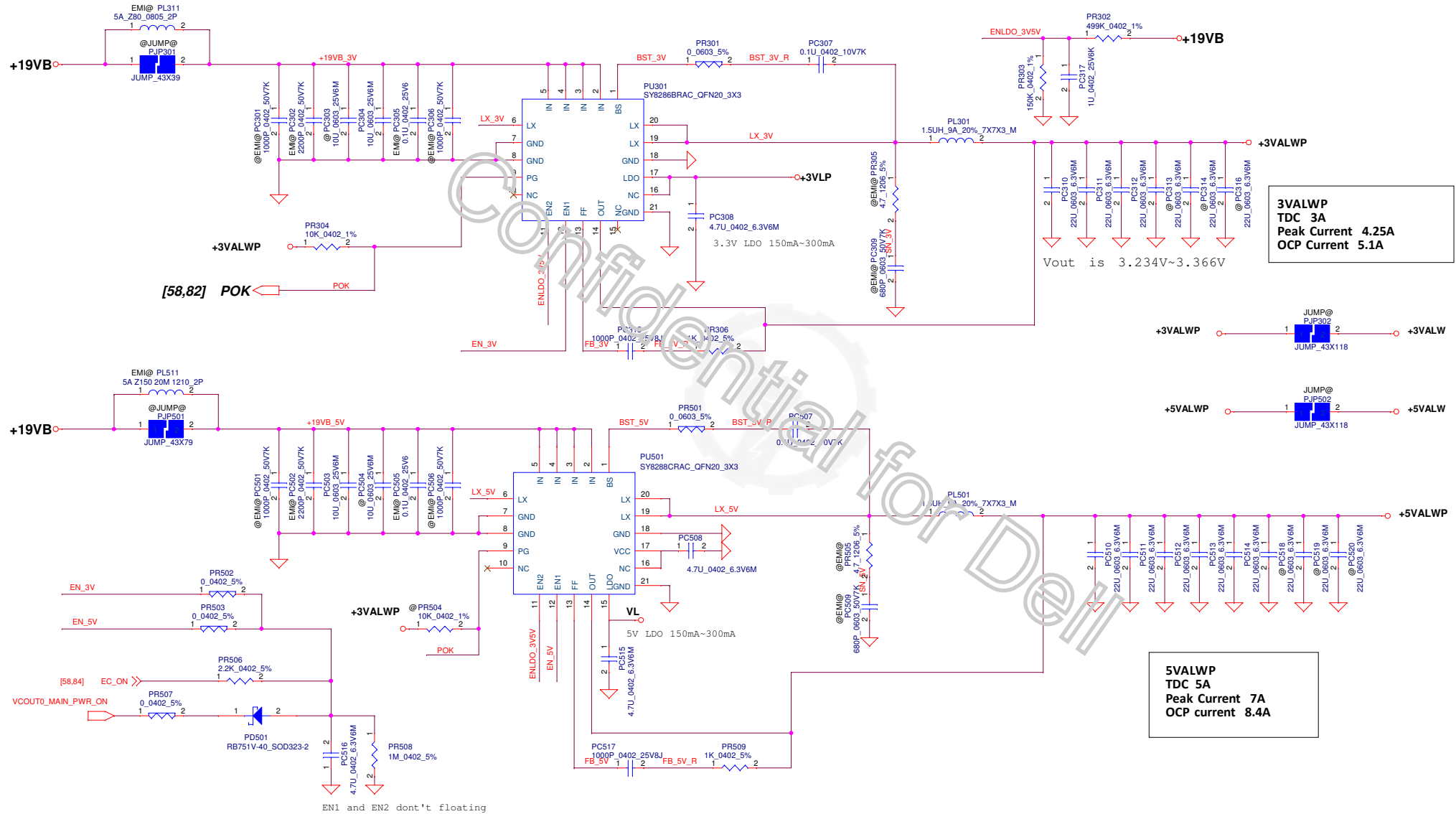
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PWR_DCIN/BATT_CONN/IOTP

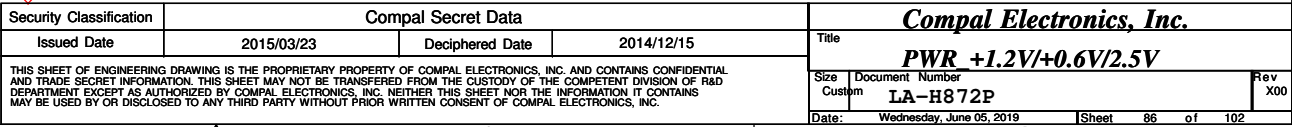
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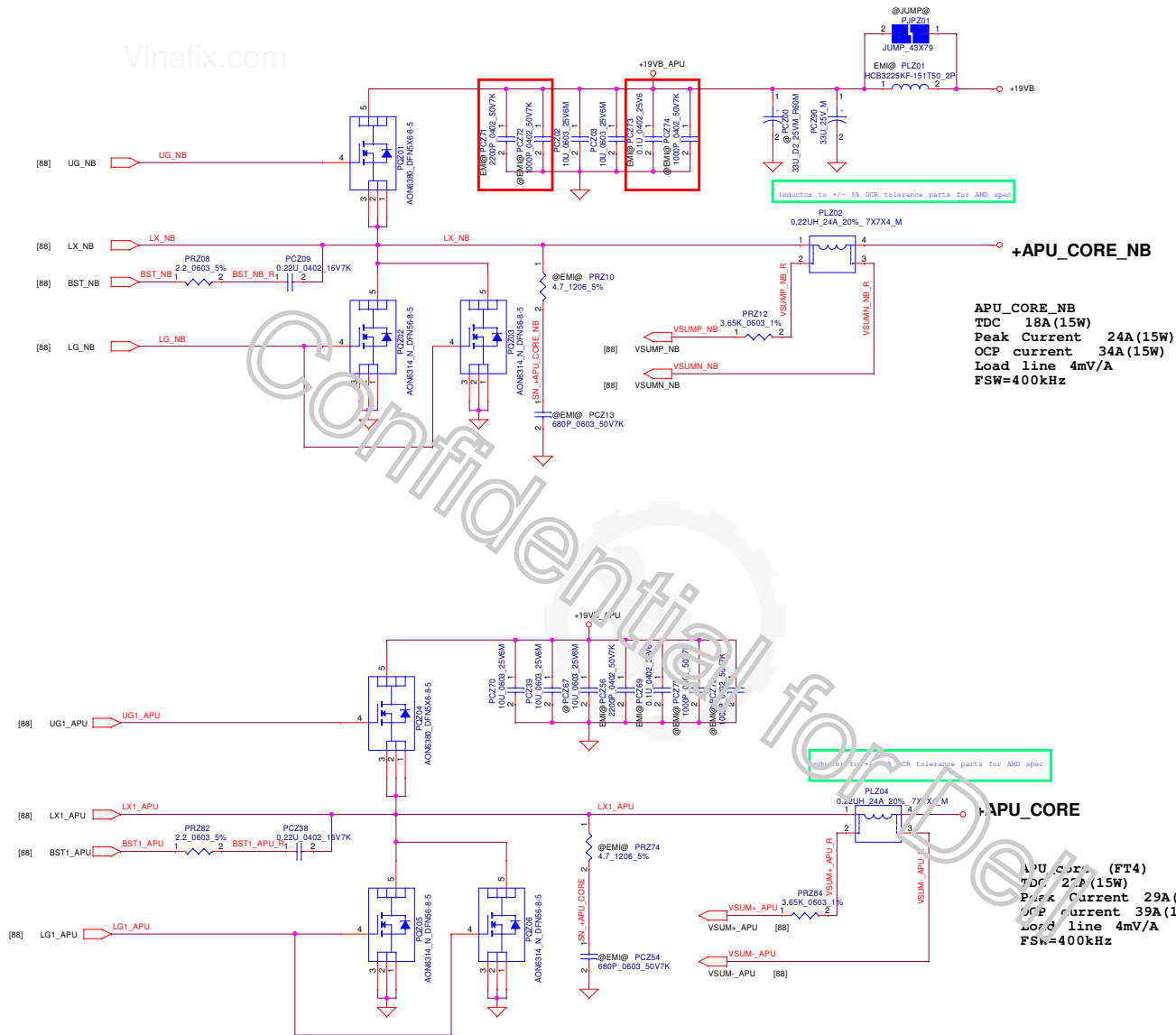
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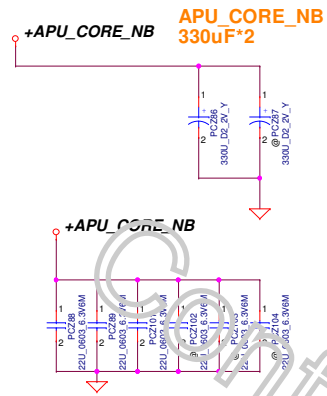
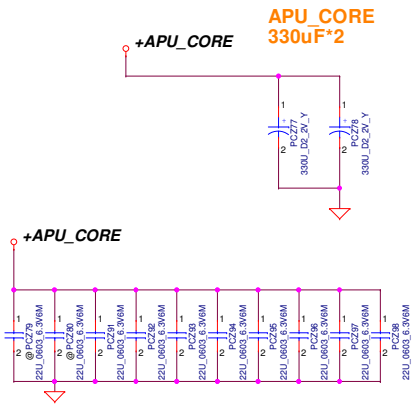
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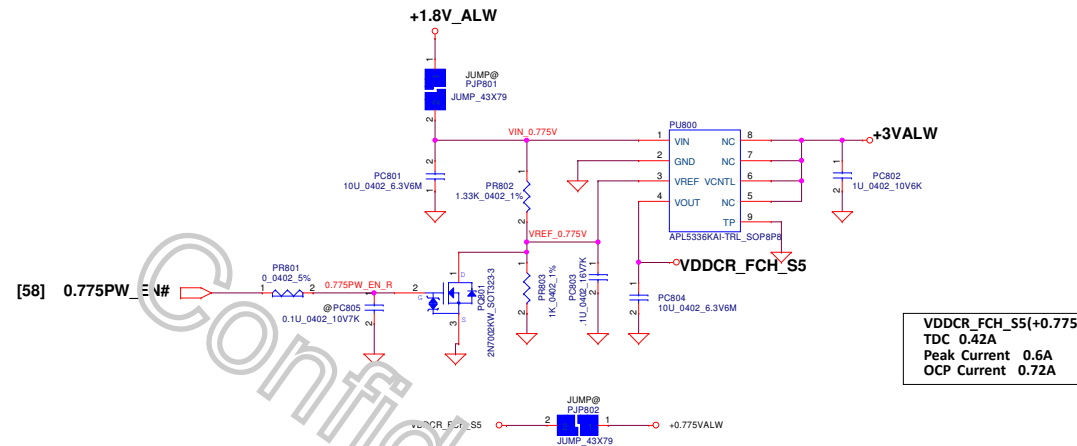


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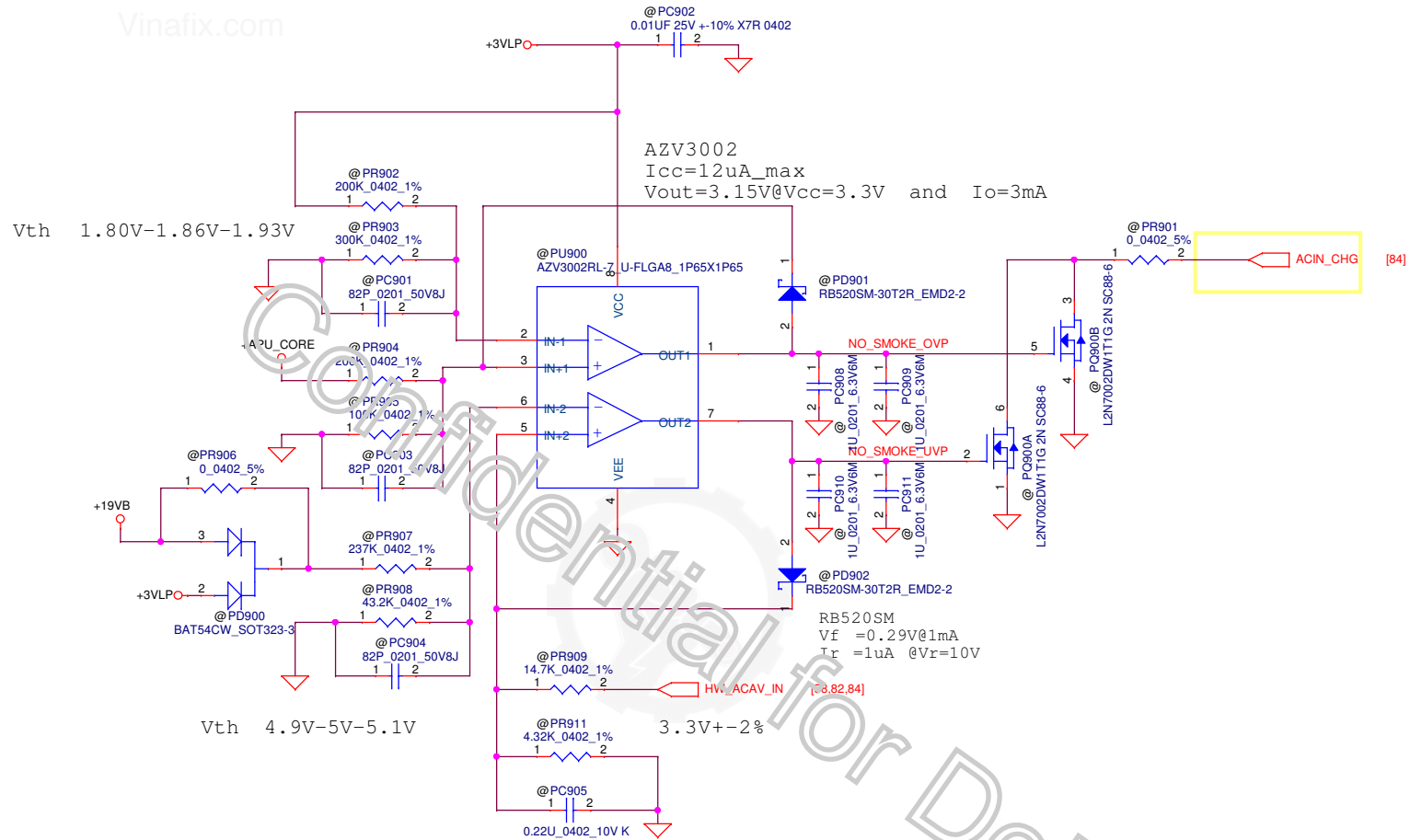
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